USB Core
Application Note

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General Information

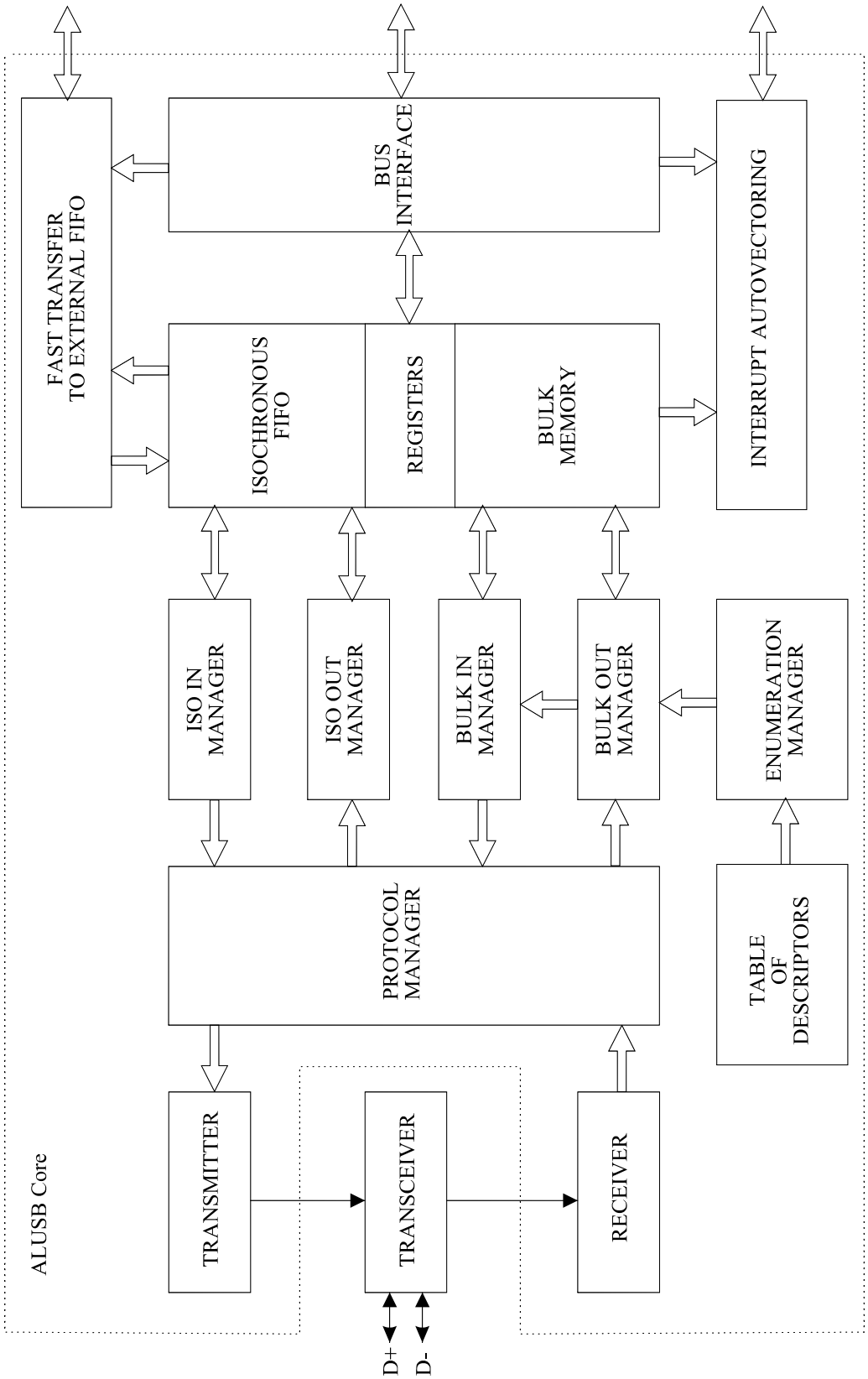
Aldec USB core is the VHDL model of USB Function Controller which is fully compatible with the USB 1.1 specification. The core has been optimized for popular FPGA devices and its functionality has been verified in the real hardware.

Features

- Fully compliant to USB 1.1 specification
- Software and hardware verified (VCC Workbench)
- Supports full-speed 12Mbps
- Support for bulk/interrupt transfers
- Up to 14 Bulk endpoints excluding control endpoint zero
- Maximum Packet Size for bulk endpoints
- Support for isochronous transfer
- Up to 16 isochronous endpoints
- Optionally Maximum Packet Size for isochronous endpoint
- Hardware enumeration manager
- Optionally fast DMA transfer mode for external isochronous FIFO
- Optionally support for interrupt autovectoring

Block Diagram

The USB core is divided into modules as shown on figure below. The Transmitter and Receiver modules handle NRZI decoding/encoding, CRC generation and checking, and bit–stuffing. It also provides interface signals for an external transceiver. The Protocol Manager handles endpoint address decoding for USB packets. Each Endpoint Manager is informed by the Protocol Manager if a token addressed to the endpoint has been received. The Endpoint Managers handle communication between Receiver/Transmitter and endpoint memory (Bulk Memory or Isochronous FIFO). The USB core contains additional module named Enumeration Manager. This unit handles the enumeration process when the device is first plugged in. The Enumeration Manager can be turned off and the enumeration process may be handled by 8051 microcontroller. The Bulk Memory buffer is a part of the 8051 address space as well as control registers. The Isochronous FIFO buffer is located outside the 8051 address space. Optionally, the USB core provides fast DMA transfer between external FIFO and Isochronous FIFO memory. Interrupt autovectoring is also supported optionally. This module automatically supplies autovector for each USB interrupt. The 8051 microcontroller does not have to test bits to determine the source of the interrupt.



Simplified Block Diagram

Implementation Data

The core has been synthesized and implemented to different types of reprogrammable devices. The model has been verified using the simulation environment and tested on the real hardware.

Configuration	Gate Count
16 Bulk Endpoints	20k + 1kB RAM
16 Bulk Endpoints + Hardware Enumeration	25k + 1kB RAM
16 Bulk Endpoints + 16 Isochronous Endpoints	46.5k + 3kB RAM
16 Bulk Endpoints+16 Isochronous Endpoints + Hardware Enumeration	52K + 3kB RAM

Deliverables

After you request the desired compiled synthesizable core, Aldec delivers the following files:

- Both technology-dependent EDIF (USB_CORE.EDF) and VHDL (USB_CORE.VHD) netlists
- User-Guide and Application Notes

Usually Aldec delivers both EDIF and VHDL netlists for customers who order the synthesizable model. The EDIF netlist is used for the place and route process and VHDL is the post-synthesis netlist used for the simulation only. Of course, both netlists are technology-dependent, because they are created after the synthesis where the customer needs to specify a vendor, target family, etc.

Aldec can provide also a set of VHDL test benches for their cores. Usually they are sold at the additional charge.

Source codes are sold on a case-by-case basis.